What is Claimed is:

1. In an apparatus for arbitrating data transmission between a first and second devices corresponding to a media access control (MAC) device and a physical layer (PHY) device having a serial media independent interface (SMII), respectively,

the apparatus comprising:

at least one buffering means for buffering transmission data input from the first device to be resynchronized a predetermined number of times in a unit of a segment and outputting the resynchronized transmission data to the second device.

2. The apparatus for arbitrating data transmission amongst devices having SMII standard as recited in claim 1,

the apparatus further comprising at least one clock phase selecting means, connected to a clock input end of the buffering means, for varying phases of clocks input in predetermined ratios and supplying the varied clocks to the clock input end.

3. The apparatus for arbitrating data transmission amongst devices having SMII standard as recited in claim 1,

the apparatus further comprising at least one switching means, positioned between output ends of the buffering means and the second device, for switching

output paths of the buffering means and sending the transmission data, output from the output end of the buffering means with delayed for a predetermined number of clocks, to the second device.

4. The apparatus for arbitrating data transmission amongst devices having SMII standard as recited in claim 2,

the apparatus further comprising at least one switching means, positioned between output ends of the buffering means and the second device, for switching output paths of the buffering means and sending the transmission data, output from the output end of the buffering means with delayed for a predetermined number of clocks, to the second device.

5. In an apparatus for arbitrating data transmission between a media access control (MAC) device and a physical layer (PHY) device having a serial media independent interface (SMII),

the apparatus comprising:

a first buffer for buffering receiving data, input from the PHY device in a unit of a segment, to be resynchronized a predetermined number of times and outputting the resynchronized receiving data to the MAC device;

a second buffer for buffering transmitting data, input from the MAC device in a unit of a segment, to be resynchronized a predetermined number of times and

outputting the resynchronized transmitting data to the PHY device; and

a third buffer for buffering synchronization signals, input from the MAC device every segment, to be resynchronized a predetermined number of times and outputting the resynchronized synchronization signals to the PHY device.

6. The apparatus for arbitrating data transmission amongst devices having SMII standard as recited in claim 5,

wherein the first to third buffers include a plurality of output ends for outputting transmitting/receiving data and synchronization signals, respectively, with delayed for a predetermined number of clocks,

the apparatus further comprising;

a first clock switch for switching output paths of the first buffer and forwarding receiving data, output from the output end of the first buffer, to the MAC device;

a second clock switch for switching output paths of the second buffer and forwarding transmitting data, output from the output end of the second buffer, to the PHY device; and

a third clock switch for switching output paths of the third buffer and forwarding synchronization signals, output from the output end of the third buffer, to the PHY device.

7. The apparatus for arbitrating data transmission amongst devices

having SMII standard as recited in claim 5,

the apparatus further comprising at least one clock phase selector, connected to each clock input end of the first to third buffers selectively, for varying phases of clocks input in predetermined ratios and supplying the varied clocks to the clock input end.

8. The apparatus for arbitrating data transmission amongst devices having SMII standard as recited in claim 6,

the apparatus further comprising at least one clock phase selector, connected to each clock input end of the first to third buffers selectively, for varying phases of clocks input in predetermined ratios and supplying the varied clocks to the clock input end.

9. The apparatus for arbitrating data transmission amongst devices having SMII standard as recited in claim 7,

wherein the number of times for resynchronizing process is set one to ten.

10. The apparatus for arbitrating data transmission amongst devices having SMII standard as recited in claim 7,

wherein the operations of selecting the clock phase by means of the clock phase selector, and switching the output paths of the first to third buffers by means

of the first to third clock switches, are executed by at least one DIP switch.

11. The apparatus for arbitrating data transmission amongst devices having SMII standard as recited in claim 7,

wherein the operations of selecting the clock phase by means of the clock phase selector, and switching the output paths of the first to third buffers by means of the first to third clock switches, are executed by a control means including a storing means storing a predetermined phase information of the clock varied based on a physical status of a system, the control means figuring out how much delays occur between the transmitting/receiving data and the synchronization signals.

12. In a method for arbitrating data transmission between a first and a second devices corresponding to a media access control (MAC) device and a physical layer (PHY) device having a serial media independent interface (SMII), respectively,

the method comprising:

buffering transmission data input from the first device to be resynchronized a predetermined number of times in a unit of a segment having a predetermined number of clocks;

switching output paths to output the buffered transmission data with delayed for a predetermined number of clocks; and

forwarding the delayed transmission data to the second device.

13. The method for arbitrating data transmission amongst devices having SMII standard as recited in claim 12,

wherein the transmission data includes transmitting, receiving data and synchronization signals, and

wherein the number of times for resynchronizing process is set one to ten.